



Application No. 10/681,833  
Attorney Docket: CPAC 1029-4

**CERTIFICATE OF MAILING**

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*Paula Faulk Hurley*  
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: Marcos Karnezos	Attorney Docket No.: CPAC 1029-4
Application No.: 10/681,833	Examiner: Pershelle L. Greene
Filed: October 8, 2003	Group: 2826
Title: Semiconductor Stacked Multi-Package Module Having Inverted Second Package and Electrically Shielded First Package	Confirmation No.: 6605
	Customer No. 22470

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**SUBMISSION OF PRIOR ART AFTER NOTICE OF ALLOWANCE**

Sir:

Applicants submit the below-listed documents to be placed in the file:

- Karnezos; U.S. Patent No. 6,838,761 issued 04 January 2005 for "Semiconductor multi-package module having wire bond interconnect between stacked packages and having electrical shield".
- Karnezos; U.S. Patent No. 6,906,416 issued 14 June 2005 for "Semiconductor multi-package module having inverted second package stacked over die-up flip-chip ball grid array (BGA) package".
- Halahan; U.S. Patent No. 6,787,916 issued 07 September 2004 for "Structures having a substrate with a cavity and having an integrated circuit bonded to a contact pad located in the cavity".
- Choi III; U.S. Patent No. 6,864,566 issued on 08 March 2005 for "Duel die package".

- Baek et al.; U.S. Patent 6,835,598 issued on 28 December 2004 for "Stacked semiconductor module and method of manufacturing the same".
- Hynix Semiconductor, Inc.; KR 2004085348A for "Chip stack package", published on 08 October 2004.
- Hitachi Ltd.; JP 2001223326A for "Semiconductor device", published on 17 August 2001.

Respectfully submitted,

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Date: 15 August 2005

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